CLAIMS

What is claimed is:

1. A method for providing a power enhanced lateral DMOS device comprising the steps of:

(a) providing a semiconductor substrate with a plurality of source/body structures thereon;

(b) providing a slot in the semiconductor substrate between the plurality of source/body structures to provide a truncated source; and

(c) providing a metal within the slot to provide a ground strap device.

2. The method of claim 1 wherein the semiconductor substrate providing step (a) further comprises:

(a1) providing a substrate region;

(a2) providing an epitaxial (EPI) layer over the substrate region; and

(a3) etching a plurality of source body structures in the EPI layer.

3. The method of claim 1 wherein the truncated source and the ground strap reduce voltage drop in the body to ground due to current in the body as a result of impact ionization in the source/body junction.

4. The method of claim 1 wherein snap back voltage is enhanced due to a higher breakdown voltage due to reduced NPN action in the ground/body/epitaxial parasitic transistor.

5. The method of claim 1 wherein the at least one slot providing step (b) includes the step of (b1) oxidizing the at least one slot.

6. The method of claim 2 wherein the at least one slot proving step (b) comprises (b1) providing the slot to the surface of the EPI layer.

7. The method of claim 1 wherein the at least one metal providing step (c) comprises the step of:

(c1) filling the slot utilizing a metal that is provided on the surface of the field oxide that is composed of two metal depositions, each of which is of a thickness that is one-half the depth or width of the at least one slot..

8. The method of claim 1 wherein the structure is oxide isolated.

9. The method of claim 1 wherein the metal comprises a first and second metal that can be provided with single metal patterning and etching.

10. The method of claim 9 wherein the first and second metals can be thick.

11. A power enhanced lateral DMOS device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of source/body structures thereon; and

a slot on the semiconductor substrate between the plurality of source/body

structures to provide a truncated source, the slot oxidized, and

a metal within the slot to provide a ground strap shorting the source to body to ground.

12. The LDMOS device of claim 11 wherein the semiconductor substrate comprises:

a substrate region; and a buried layer, or Boron Up Diffusion where required and

an epitaxial (EPI) layer over the substrate region, wherein the source/body structures are provided in the EPI layer.

13. The LDMOS device of claim 11 wherein the truncated source and the ground strap shortens the path from the source/body junction to ground and reduces voltage drop that occurs as a result of current flow induced by impact ionization in the source/body junction.

14. The LDMOS device of claim 11 wherein snap back voltage is enhanced to a higher breakdown voltage due to reduced NPN action in the ground/body/epitaxial parasitic NPN transistor.

15. The LDMOS device of claim 11 wherein the structure is oxide isolated.

16. The LDMOS device of claim 11 wherein the metal comprises a first and second metal that can be provided with single metal patterning and etching for the interconnect.

17. The LDMOS device of claim 16 wherein the first and second metals can be thick as compared to standard approaches which would result in metal breakage.